the gate oxide layer, spacers formed beside the gate on the gate oxide layer, and doped source/drain (S/D) regions arranged on respective sides of a gate conductor. The gate is separated from a channel (which is situated between the S/D regions) by the gate oxide layer. Shallow trench insulator (STI), local oxidation of silicon (LOCOS), or poly-buffered LOCOS isolations are usually employed to provide for isolation of adjacent transistors. When the FET is operated, an electric field is generated by applying a voltage to the gate. The electrical field is used to control the channel situated between the S/D regions. For example, if the channel is turned on, the electrons flow from the source region to the drain region. In contrast, if the channel is turned off, the electrons cannot flow between the source region and the drain region. Therefore, the on or off state of the channel controls the connection or disconnection of the circuit.

Please amend the paragraph beginning on page 19, line 4 and extending through line 18, as follows:

As depicted in FIGS. 6a - 6b, step 108 of method 100 is to form gate conductor layer 212 overlying hard mask film 208 narrow lines, oxide layers 210, and buried insulator 204. Gate conductor layer 212 may be any suitable conducting material, typically a polycrystalline silicon material, although amorphous silicon, a combination of amorphous silicon and polysilicon, polysilicon-germanium, or any other appropriate material may be used to form gate conductor layer 212. In addition, in some embodiments of the present invention, it might be advantageous to employ a metal gate conductor layer 212, such as W, Mo, or Ta, or any other refractory metal, or alternatively, a silicided gate conductor comprising polysilicon added with Ni or Co. In step 108, where gate conductor layer ~~214~~ 212 encompasses a silicon material, such layers may be

deposited as a doped layer (in-situ doping). Where gate conductor layer ~~214~~ 212 is a metal layer, such layers may be deposited using physical vapor or chemical vapor deposition methods or any other technique known in the art. In this manner, gate structures are formed adjacent to oxide layers 210 formed on opposing vertical sidewalls 207 of the fins formed by semiconductor layer 206 portions.

Please amend the paragraph beginning on page 21, line 1 and extending through line 14, as follows:

The FinFET embodiments of FIGS. 7a - 7b or any other Fin FET embodiments of the present invention utilizing different crystal planes for FET current channels, may be completed according to step 112 of method 100. Accordingly, exposed portions of the fins may be doped to form S/D regions. The S/D regions may define, in semiconductor layer ~~208~~ 206 portions comprising the fin bodies, channel regions underlying the gate stacks. Formation of the S/D regions may be accomplished using any of the variety of methods that have been developed to form S/D regions and that are tailored for specific performance requirements. There are many such methods for forming S/D regions having various levels of complexity. Thus, in some embodiments of the present invention, using ion implantation for example, lightly doped S/D regions or other S/D regions may be formed. Thus, for NFETs, typically P, As, or Sb for example is used for the S/D implants in the range of 1 to 5 keV and a dose of 5×10^{14} to 2×10^{15} cm^{-3}. Similarly, for PFETs, typically B, In, or Ga for example is used for the S/D implants in the range of 0.5 to 3 keV and dose of 5×10^{14} to 2×10^{15} cm^{-3}.